Claims

What is claimed is:

1. An apparatus comprising:

first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, the processing circuits performing the sampling function utilizing at least one clock signal;

a logic circuit coupled to outputs of each of the first, second and third processing circuits, and operative to generate a control signal indicative of the presence or absence of a desired relationship between the at least one clock signal and the first, second and third versions of the given signal; and

a selection circuit having an input coupled to an output of the logic circuit, wherein the selection circuit is responsive to the control signal to alter a relationship between the at least one clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship.

2. The apparatus of claim 1 wherein the desired relationship comprises a desired voltage amplitude relationship.

3. The apparatus of claim 1 wherein the desired relationship comprises a desired frequency relationship.

4. The apparatus of claim 1 wherein the desired relationship comprises a desired phase relationship.

5. The apparatus of claim 1 wherein the given signal comprises a receive data clock delivered from a deserializer circuit, and wherein the receive data clock is to be synchronized to the at least one clock signal.

6. The apparatus of claim 1 wherein the at least one clock signal comprises a clock signal associated with a first chip, and the given signal comprises a receive data clock synchronous with another clock signal associated with a second chip.

7. The apparatus of claim 1 wherein the first, second and third versions of the given signal comprise an early version, a middle version and a late version of the given signal, wherein the middle version corresponds to the early version delayed by a first amount of time, and the late version corresponds to the middle version delayed by a second amount of time.

8. The apparatus of claim 7 wherein the first and second amounts of time are substantially the same, such that the middle version of the given signal has a transition edge which is located approximately midway between a corresponding transition edge in the early and late versions.

9. The apparatus of claim 1 wherein the first, second and third versions of the given signal are generated by clocking each of at least a subset of the first, second and third versions with a different delayed version of either the at least one clock signal or another clock signal which is synchronous with the at least one clock signal.

10. The apparatus of claim 1 wherein each of the first, second and third processing circuits comprises a series-connected set of flip-flops, with each of the flip-flops in the series connection of flip-flops clocked by the clock signal, and wherein the sampling function in each of the first, second and third processing circuits comprises clocking the respective first, second and third versions of the given signal through the corresponding series-connected set of flip-flops.

11. The apparatus of claim 10 wherein the logic circuit receives an output signal from each of the series-connected sets of flip-flops, and generates the control signal based on whether or not the output signals have the same logic value within a designated sample window.

12. The apparatus of claim 1 wherein the logic circuit comprises a decision logic block for determining the presence or absence of the desired relationship, and a counter circuit which is incremented or decremented when the decision logic block determines that the desired relationship is absent, and wherein the control signal corresponds to an output of the counter circuit.

13. The apparatus of claim 1 wherein the logic circuit comprises a decision logic block for determining the presence or absence of the desired relationship, and a latch circuit which is set or reset when the decision logic block determines that the desired relationship is absent, and wherein the control signal corresponds to an output of the latch circuit.

14. The apparatus of claim 1 wherein the logic circuit and the selection circuit form at least a portion of a closed loop control system for maintaining the desired relationship between the clock signal and the first, second and third versions of the given signal.

15. An apparatus comprising:

a first chip having a first signal associated therewith;

a second chip having a second signal associated therewith, wherein the first and second signals are asynchronous;

a serializer circuit associated with the first chip;

a deserializer circuit associated with second chip and having an input coupled to an output of the serializer circuit via an interconnect; and

a synchronizer circuit associated with the second chip and having an input coupled to an output of the deserializer circuit, the synchronizer circuit comprising:

first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of an output of the deserializer synchronous with the first signal, the processing circuits performing the sampling function utilizing at least the second signal;

a logic circuit coupled to outputs of each of the first, second and third processing circuits, and operative to generate a control signal indicative of the presence or absence of a desired

phase relationship between the second signal and the first, second and third versions of the deserializer output; and

a selection circuit having an input coupled to an output of the logic circuit, wherein the selection circuit is responsive to the control signal to alter a phase relationship between the second signal and the first, second and third versions of the deserializer output if the control signal indicates the absence of the desired phase relationship.

16. A method of processing signals, the method comprising the steps of:

performing a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, utilizing at least one clock signal;

generating a control signal indicative of the presence or absence of a desired relationship between the at least one clock signal and the first, second and third versions of the given signal; and

altering a relationship between the at least one clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship.

Sub A1

17. An apparatus comprising:

first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, the processing circuits performing the sampling function utilizing a second signal to which the given signal is to be synchronized; and

a feedback control circuit having an input coupled to outputs of each of the first, second and third processing circuits, and operative: (i) to generate a control signal indicative of the presence or absence of a desired phase relationship between the second signal and the first, second and third versions of the given signal, and (ii) to alter a phase relationship between the at least one clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired phase relationship.

18. An apparatus comprising:

first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, the processing circuits performing the sampling function utilizing a second signal to which the given signal is to be synchronized; and

a feedback control circuit having an input coupled to outputs of each of the first, second and third processing circuits, wherein the feedback control circuit is operative to maintain a desired relationship between the second signal and the first, second and third versions of the given signal based on sample values generated at the outputs of the first, second and third processing circuits.